THE
JIM WILLIAMS
PAPERS

High-speed amplifiers with low offset and drift

Amplifiers designed for wide bandwidth or fast settling often exhibit inferior characteristics at dc—that is, high voltage, current offset, and drift. Used with care, the techniques described here let you build circuits that exhibit exemplary performance from dc to MHz.

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Often, you must produce an amplifier circuit that has both the low offset of a dc amplifier and the wide bandwidth of a fast device. A number of techniques let you achieve such a result. Which method is best depends heavily on your application. Several circuits follow that you can study, build, and compare to determine what's best for you.

Fig 1 shows a composite amplifier that consists of an LT1097 low-drift device (IC_1) and an LT1191 high-speed amplifier (IC_2). The overall circuit is a unity-gain inverter that has its summing node at the junction of the two 1-kΩ resistors. IC_1 monitors this summing node, compares it to ground, and drives IC_2's positive input to complete a dc-stabilizing loop around IC_2. The 100-kΩ·0.01-μF time constant at IC_1 limits the amplifier's response to low-frequency signals. IC_2 handles high-frequency inputs, whereas IC_1 stabilizes the dc operating point. The 4.7-kΩ/220Ω divider at IC_2's input prevents excessive overdrive during startup. This circuit combines IC_1's 35-μV offset and 1.5-μV/°C drift with IC_2's 450V/μsec slew rate and 90-MHz bandwidth. Bias current, dominated by IC_2, is about 500 nA.

Fig 2 is similar, except that the sensing is differential, preserving access to both of the fast amplifier's inputs. IC_1 measures the dc error at IC_2's input terminals and biases IC_2's offset pin to force the offset to within 50 μV. IC_2's offset-pin biasing arrangement always lets IC_1 find the servo point. The 0.01-μF capacitor rolls off IC_1's gain at low frequencies, and IC_2 han-

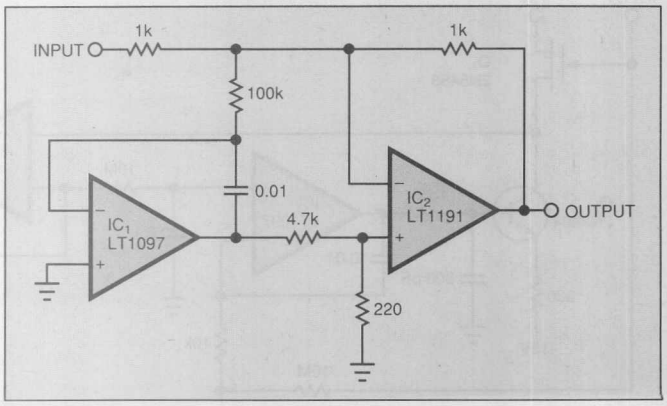

Fig 1—An integrator (IC_1) reduces the drift of a wideband amplifier (IC_2) by applying a signal to the wideband amplifier's noninverting input. That signal holds the wideband amplifier's summing junction at ground.

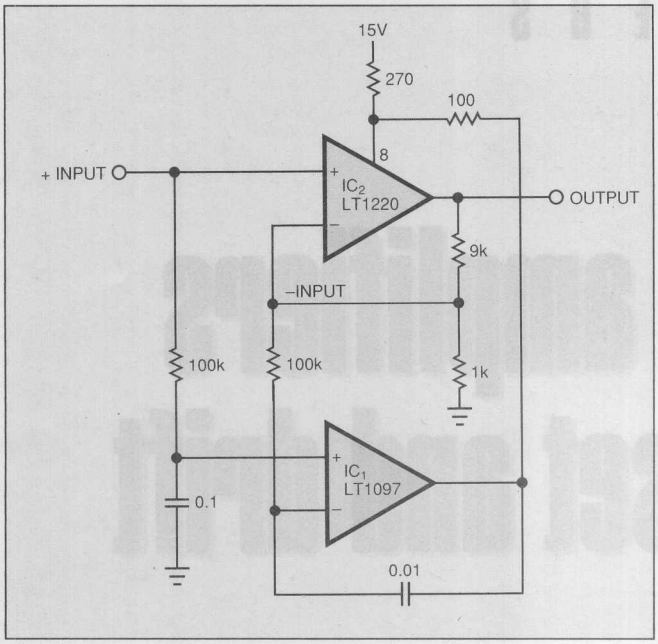

***Fig 2—You can also stabilize the offset** of a wideband amplifier (IC_2, in this case) by using a precision dc amplifier (IC_1) to apply correcting signals to the wideband amplifier's offset-trim adjustment pin.*

dles high-frequency signals. The combined characteristics of these amplifiers yield an offset voltage of 50 μV, an offset drift of 1 μV/°C, a slew rate of 250 V/μsec, and a gain bandwidth of 45 MHz.

Fig 3 shows wideband, highly stable gain-of-10 amplifier with high input impedance. The input capacitance is about 3 pF. Because of its low input capacitance and low (100 pA) bias current, the circuit is well suited for use in probing IC wafers or as a pin amplifier in automatic-test systems.

Q_1 and Q_2 constitute a simple, high-speed FET-input buffer. Q_1 functions as a source follower, and the Q_2 current-source load sets the drain-to-source channel current. IC_2 provides a gain of 10 with 100-MHz bandwidth. Normally, this open-loop configuration would drift unacceptably because there is no dc feedback. IC_1, by comparing the filtered circuit output to a similarly filtered version of the input signal, provides the feedback to stabilize the circuit. The amplified difference between these signals sets Q_2's bias—and hence Q_1's channel current—thereby forcing Q_1's V_{GS} to match the circuit's input and output potentials. The capacitor around IC_1 provides stable loop compensation. The R-C network in IC_1's output prevents that output from seeing high-speed edges coupled through Q_2's collector-base junction.

Fig 4a shows a way to combine wide bandwidth with true differential inputs and dc stabilization. IC_1 and IC_2 sense the input differentially at gains of 10. Wideband amplifier IC_1 feeds high-frequency signals to output amplifier IC_3 via a highpass network. Low-frequency and dc information get to IC_3 via the slower IC_2. The 2-kΩ/200-pF lowpass networks remove the input signal's high-frequency components, so only lower frequencies reach IC_2. Because the gain and bandwidth of the high- and low-frequency paths complement each other, IC_3's output is an undistorted, amplified version of the input (see **Fig 4b**, trace D.)

Fig 4b, trace A is one side of a differential input signal applied to the circuit. Trace B is IC_1's output

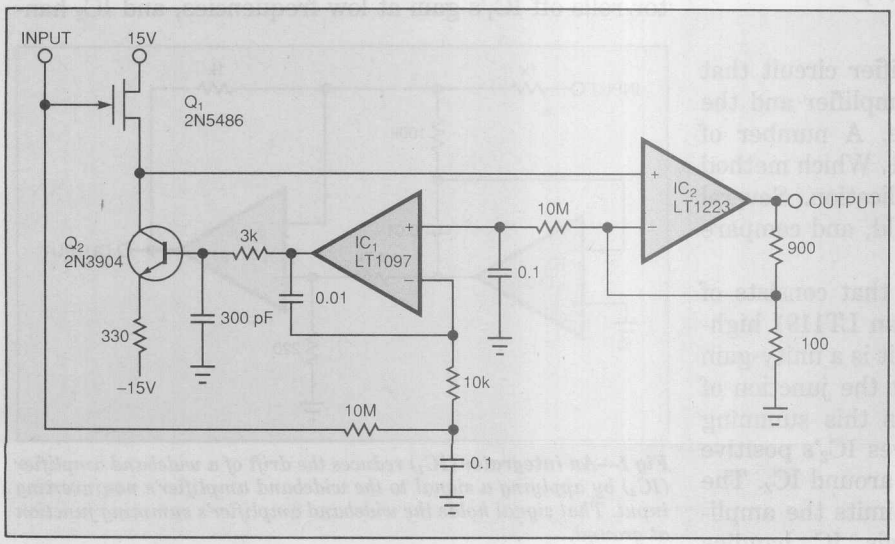

***Fig 3—An integrator (IC_1)** drives a current source (Q_2), which biases a FET (Q_1) that completes a dc feedback loop around IC_2 to stabilize the amplifier's operation at dc.*

taken at the junction of the 500Ω potentiometer and 0.001-μF capacitor. Trace C is IC_2's output. With the "ac-gain" and "dc-gain-match" trims properly adjusted, the two paths' contributions match up and trace D is clean, with no residual artifacts. You can optimize the adjustments by trimming the ac gain for the squarest corners and the dc-gain match for a flat top. Bandwidth for this circuit exceeds 35 MHz; slew rate is 450V/μsec; and dc offset is about 200 μV.

Parallel paths yield the best of two worlds

Fig 5a shows a very powerful extension of the previous circuit. The circuits operate similarly, but this one has a gain of 1000; its bandwidth is about 35 MHz; its rise time is 7 nsec; and its delay is less than 7.5 nsec. Full-power response is available to 10 MHz, and broadband input noise is about 15 μV. This kind of speed, coupled with true differential inputs, a gain of 1000, high dc stability, and low cost make the circuit broadly applicable in wideband instrumentation.

As before, two differential amplifiers, IC_1 and IC_2, simultaneously sense the inputs. In this case, IC_1 is a 592-733 type operating at a gain of 100. Its differential outputs feed output amplifier IC_3 via 1-μF/1-kΩ high-pass networks that strip out the dc content of IC_1's output. IC_2, a precision dc differential amplifier, operates in similar fashion to its counterpart in the previous circuit, supplying dc and low-frequency information to IC_3 at a trimmed gain of 100.

In this case, the output amplifier, IC_3, is not a follower but a differential-input/single-ended-output gain block whose nominal gain is 10. This change is necessary because IC_1's differential output must become a single-ended signal to provide the circuit's final output. Consequently, IC_2 does not directly apply its low-frequency information to IC_3 as it did before. Instead, IC_4 measures the difference between IC_2's output and a fraction of IC_3's output. IC_4's output, biasing IC_3's positive input via the 1-kΩ resistor, closes a loop around the circuit's dc and low-frequency path. To make the circuit's dc gain equal to its ac gain, you adjust the divider that feeds IC_4's negative input.

Fig 5b shows the circuit's response to a 60-nsec, 2.5-mV pulse, trace A. The ×1000 output, trace B, responds cleanly, with both delay and rise time in the 5- to 7-nsec range. Some small amount of overshoot is evident, but you can trim the overshoot with the peaking adjustment at IC_1. **Fig 5c** plots the circuit's gain vs frequency. The gain is flat within 0.5 dB to 20 MHz, with the −3 dB point at 40 MHz. The overshoot of **Fig 5b** shows up here as a very slight gain increase starting around 1 MHz and continuing to about 15 MHz. The peaking adjustment eliminates this effect.

To use this circuit, apply a low-frequency or dc signal of known amplitude and adjust the low-frequency gain to ×1000 after the output has settled. Next, adjust the high-frequency gain so that the signal's leading and trailing corners have amplitudes identical to those

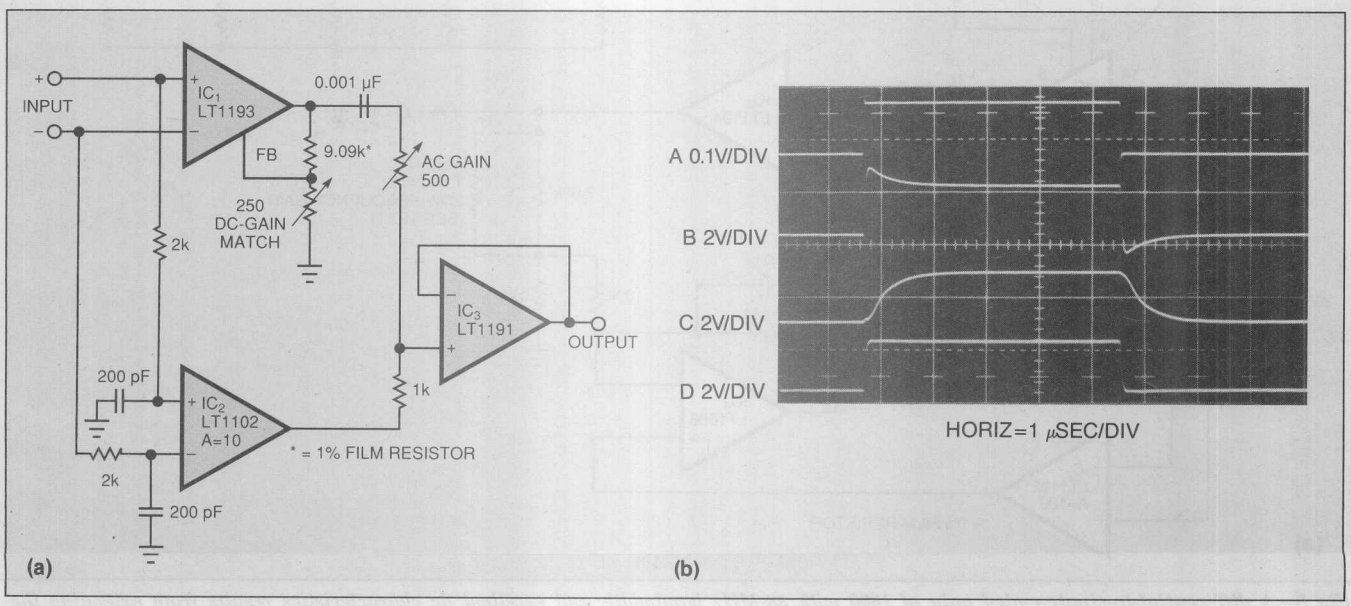

***Fig 4—Parallel paths** for ac and dc signals **(a)** provide low offset and good dynamic response—if you correctly adjust the trims (**b**, trace D).*

of the settled portion. Finally, trim the peaking adjustment for the best settling of the output pulse's corners.

Fig 5d shows the input (trace A) and output (trace B) waveforms with all adjustments properly set. The fidelity is excellent, with no aberrations or other artifacts of the parallel-path operation evident. **Fig 5e** shows the effects of too much ac gain; excessive peaking on the edges, with proper amplitude achieved only after the dc channel takes control of the output. Similarly, excessive dc gain produces **Fig 5f**'s traces. The ac-gain path provides proper initial response, but too much dc gain forces a long, tailing response that finally settles at an incorrect amplitude.

The use of parallel-path schemes to simultaneously achieve wide bandwidth and outstanding dc performance isn't new. In fact, it predates the use of low-drift bipolar differential gain stages. The first parallel-path amplifiers achieved dc stability by using electromechanical choppers to convert dc to ac. Gain stages consisting first of vacuum tubes and later of Germanium transistors amplified the chopped dc. Synchronous rectifiers converted the ac back to dc. AC-coupled amplifi-

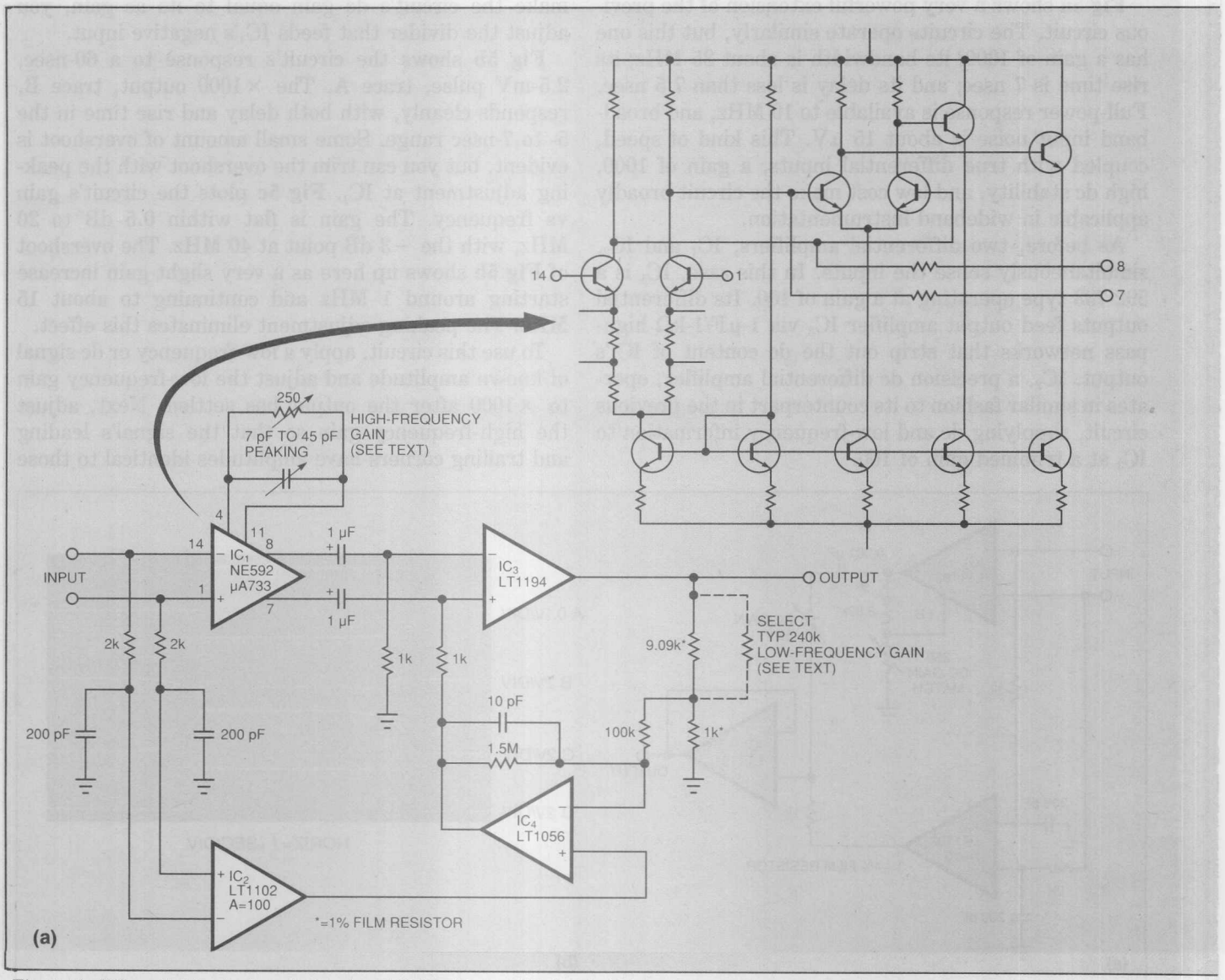

***Fig 5—A differential-to-single-ended gain of 1000** with 38-MHz bandwidth and excellent dc characteristics results from extending the parallel-path architecture, **(a)**. The pulse response (**b**, trace B) shows a minimum of overshoot, which is reflected in the frequency response*

ers in parallel with the chopper amplifiers provided good bandwidth. As **Figs 5e** and **5f** illustrate, these schemes have historically had a problem in many applications that demand the best at both dc and high frequencies: Unless you carefully match the dc and ac gains, the amplifiers' response to an input voltage step exhibits a long "tail." Keeping the response free of such tails over wide temperature ranges and long periods of time has always presented a challenge. Modern components make meeting that challenge easier, but the challenge still exists. EDN

Author's biography

For more information on this article's author, turn to page 163 in the October 10, 1991, issue.

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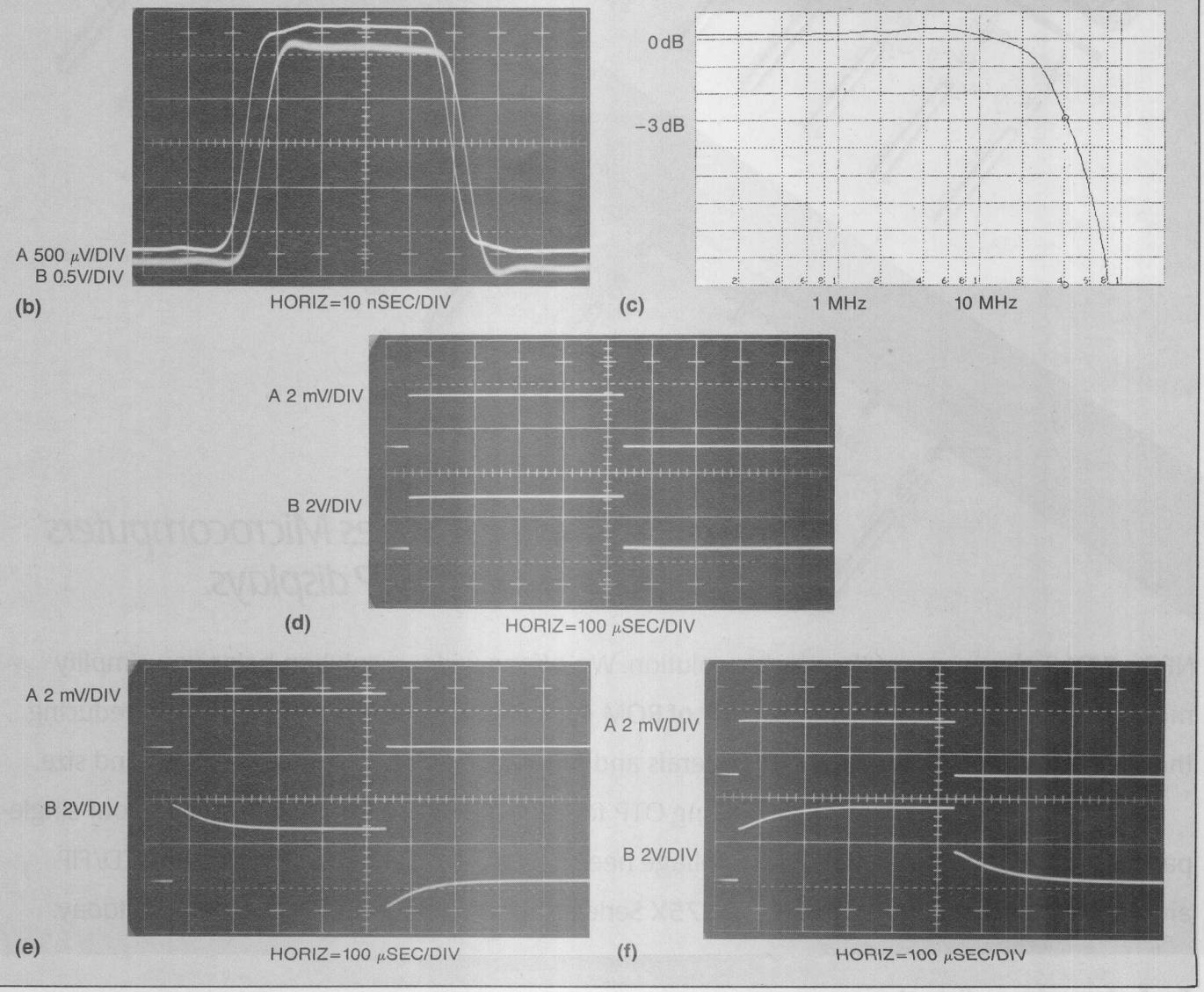

(c) as a slight peak near 6 MHz. In the other three photos, (d, e, and f), you see, respectively, the effects of correctly matching the ac and dc gains, setting the ac gain too high, and setting the dc gain too high.